Contents

Preface *vii*

Chapter 1: Introduction to Digital Systems **1.1–1.6**

1.1 Analog and Digital Electronics 1.1
1.2 Analog and Digital Signal 1.2
1.3 Binary Representation in Digital Systems 1.2
1.4 Digital Integrated Circuits (ICs) 1.3
1.5 Digital Systems 1.4
1.6 Binary Storage Devices: Registers and Memory 1.4
1.7 Binary Logic and Arithmetic 1.6
1.8 Logic Families 1.6

Chapter 2: Number Systems **2.1–2.54**

2.1 Review of Number Systems Representation and Conversions 2.1
2.1.1 Number Representation 2.2
2.1.2 Decimal Number System 2.2
2.1.3 Binary Number System 2.3
2.1.4 Octal Number System 2.7
2.1.5 Hexadecimal Number System 2.10
2.1.6 Relation between Binary, Octal and Hexadecimal Number Systems 2.13
2.2 Binary Arithmetic 2.15
2.2.1 Binary Addition 2.16
2.2.2 Binary Subtraction 2.16
2.2.3 Binary Multiplication 2.17
2.2.4 Binary Division 2.20
2.3 Unsigned and Signed Binary Number Systems 2.23
2.3.1 Unsigned Binary 2.23
2.3.2 Sign-Magnitude Form 2.24
2.3.3 Complement of Number Systems (r's and (r – 1)'s Complement) 2.25
2.3.4 One's Complement 2.26
2.3.5 Two's Complement 2.28
2.3.6 One's and Two's Complement Addition 2.30
2.3.7 One's and Two's Complement Subtraction 2.33
2.4 Nine's and Ten's Complement 2.34
2.4.1 Nine's and Ten's Complement Addition 2.36
2.4.2 Nine's and Ten's Complement Subtraction 2.39
2.5 Summary of Important Concepts 2.40

2.6 Short-Answer Questions 2.42
2.7 Exercises 2.49

Chapter 3: Binary Codes 3.1–3.64

3.1 Introduction 3.1
3.1.1 Classification of Binary Codes 3.1
3.2 BCD Codes 3.3
3.2.1 8421 BCD 3.5
3.2.2 BCD Addition 3.6
3.2.3 BCD Subtraction 3.8
3.2.4 2421 Code 3.13
3.2.5 5421 Code 3.14
3.2.6 8, 4, – 2, –1 Code 3.16
3.2.7 Excess-3 Code 3.17
3.2.8 Excess-3 Addition 3.19
3.2.9 Excess-3 Subtraction 3.21
3.3 Gray Code 3.25
3.4 Alphanumeric Code 3.30
3.4.1 ASCII Code 3.30
3.4.2 EBCDIC Code 3.33
3.5 Error Detection and Correction 3.36
3.5.1 Parity 3.36
3.5.2 Hamming Code 3.37
3.5.3 Checksum 3.50
3.6 Summary of Important Concepts 3.54
3.7 Short-Answer Questions 3.56
3.8 Exercises 3.59

Chapter 4: Boolean Algebra and Logic Gates 4.1–4.60

4.1 Boolean Algebra 4.1
4.1.1 Duality 4.2
4.1.2 Postulates of Boolean Algebra 4.2
4.1.3 Boolean Theorems 4.5
4.2 Binary Logic 4.8
4.3 Logic Gates 4.9
4.3.1 Universal Gates 4.13
4.3.2 Positive and Negative Logic Gates 4.17
4.4 Boolean Functions 4.20
4.4.1 Implementation of Boolean Functions by Logic Gates 4.23
4.4.2 Minterms 4.24
4.4.3 Maxterms 4.25
4.4.4 Standard Forms 4.26
4.4.5 Sum-of-Products and Product-of-Sums Simplification 4.27
4.4.6 Canonical Form 4.28

4.4.7 Complement of a Function 4.28
4.4.8 Implementation of Boolean Functions using Universal Gates 4.29
4.4.9 Implementation of Logic Design using Standard Logic Gate IC's 4.38
4.4.10 Implementation of Logic Design using Standard Universal Gate IC's 4.40
4.5 Summary of Important Concepts 4.43
4.6 Short-Answer Questions 4.44
4.7 Exercises 4.51

CHAPTER 5: Gate Level Minimization of Boolean Functions 5.1–5.56

5.1 Simplification of Boolean Expressions or Functions 5.1
5.2 Karnaugh Map (or K-map) Minimization 5.2
5.2.1 Realization of Sum-of-Products Form using K-map 5.2
5.2.2 Two-Variable K-map 5.3
5.2.3 Three-Variable K-map 5.5
5.2.4 Four-Variable K-map 5.8
5.2.5 Five-Variable K-map 5.11
5.2.6 Realization of Product-of-Sums Form using K-map 5.21
5.2.7 Completely and Incompletely Specified Functions (K-map with Don't-Care Conditions) 5.22
5.3 Quine-McCluskey (QM) Method of Minimization (Table Method of Minimization) 5.36
5.4 Summary of Important Concepts 5.45
5.5 Short-Answer Questions 5.46
5.6 Exercises 5.49

CHAPTER 6: Combinational Logic Circuits 6.1–6.130

6.1 Introduction 6.1
6.2 Combinational Circuits 6.1
6.2.1 K-map Representation and Minimization using K-maps 6.2
6.2.2 Problem Formulation and Design of Combinational Circuits 6.2
6.3 Code Converters 6.7
6.4 Decoders 6.16
6.4.1 Logic High 2-to-4 Decoder 6.17
6.4.2 Logic Low 2-to-4 Decoder 6.19
6.4.3 Logic High 2-to-4 Decoder with Logic High Enable 6.20
6.4.4 Logic High 2-to-4 Decoder with Logic Low Enable 6.22
6.4.5 Logic Low 2-to-4 Decoder with Logic High Enable 6.25
6.4.6 Logic Low 2-to-4 Decoder with Logic Low Enable 6.28
6.4.7 Logic High 3-to-8 Decoder 6.31
6.4.8 Logic Low 3-to-8 Decoder 6.33
6.4.9 Expanding the Decoder 6.36
6.4.10 Combinational Circuit Design using Decoder 6.40
6.4.11 Implementation of Combinational Logic Design using Standard Decoder IC's 6.46

6.5 Encoders 6.50
6.5.1 Logic High 4-to-2 Encoder 6.50
6.5.2 Logic High 8-to-3 Encoder 6.52
6.6 Priority Encoders 6.54
6.6.1 Logic High 4-to-2 Priority Encoder 6.55
6.6.2 Logic High 4-to-2 Priority Encoder Design using K-maps 6.57
6.6.3 Logic High 8-to-3 Priority Encoder 6.58
6.7 Multiplexer 6.62
6.7.1 Expanding the Multiplexer 6.67
6.7.2 Combinational Circuit Design using Multiplexer 6.74
6.7.3 Implementation of Combinational Logic Design using Standard Multiplexer IC's 6.86
6.8 Demultiplexer 6.95
6.8.1 Expanding the Demultiplexer 6.101
6.8.2 Demultiplexers and Decoders 6.102
6.9 Combinational Systems Case Study 6.103
6.9.1 Digital Trans-Receiver 6.103
6.9.2 Parallel Data Trans-Receiver 6.103
6.9.3 Serial Data Trans-Receiver 6.104
6.9.4 Parity Generator and Checker 6.105
6.9.5 BCD to 7-Segment Decoder 6.110
6.10 Summary of Important Concepts 6.116
6.11 Short-Answer Questions 6.116
6.12 Exercises 6.120

CHAPTER 7: Combinational Logic-Arithmatic Circuits 7.1–7.60

7.1 Adders 7.1
7.1.1 Half Adder 7.1
7.1.2 Full Adder 7.2
7.1.3 Binary Parallel Adder 7.10
7.1.4 Carry Look Ahead Adder 7.13
7.1.5 BCD Adder 7.16
7.2 Subtractors 7.20
7.2.1 Half Subtractor 7.20
7.2.2 Full Subtractor 7.21
7.3 Parallel Adder/Subtractor 7.26
7.3.1 Binary Parallel Adder/Subtractor 7.26
7.3.2 BCD Subtractor 7.28
7.3.3 BCD Adder/Subtractor 7.29
7.4 Magnitude Comparator 7.29
7.4.1 4-bit Magnitude Comparator 7.29
7.4.2 3-bit Magnitude Comparator 7.35
7.4.3 2-bit Magnitude Comparator 7.36

7.5 Combinational Multiplier 7.37
7.5.1 Combinational 2-bit Binary Multiplier 7.37
7.5.2 Combinational 4-bit Binary Multiplier 7.38
7.6 Arithmetic and Logic Unit 7.40
7.6.1 Design of 4-bit ALU 7.40
7.6.2 ALU using Standard IC's 7.45
7.6.3 8-bit and 16-bit ALU using 74381/382 7.45
7.6.4 8-bit and 16-bit ALU using 74181 7.48
7.7 Summary of Important Concepts 7.51
7.8 Short-Answer Questions 7.52
7.9 Exercises 7.54

CHAPTER 8: Latches and Flip-Flops 8.1–8.80

8.1 Bistable Element and Latches 8.1
8.1.1 SR Latch 8.2
8.1.2 Analysis of SR Latch using NOR Gates 8.2
8.1.3 Analysis of SR Latch using NAND Gates 8.5
8.1.4 D Latch 8.10
8.1.5 Application of Latches-Swith Debouncing 8.11
8.2 Flip-Flops 8.14
8.2.1 Clock and Triggering of Flip-Flops 8.14
8.2.2 SR Flip-Flop 8.16
8.2.3 JK Flip-Flop 8.22
8.2.4 T Flip-Flop (Toggle Flip-Flop) 8.29
8.2.5 D Flip-Flop (Data Flip-Flop) 8.31
8.2.6 Flip-Flop with Preset and Reset Facility 8.33
8.3 Master-Slave Flip-Flop 8.34
8.4 Excitation Table and Characteristic Equation of Flip-Flops 8.36
8.4.1 Excitation Table of D Flip-Flop 8.36
8.4.2 Excitation Table of JK Flip-Flop 8.38
8.4.3 Excitation Table of T Flip-Flop 8.40
8.4.4 Excitation Table of SR Flip-Flop 8.41
8.5 Conversion of Flip-Flops 8.43
8.5.1 Conversion of SR to JK Flip-Flop 8.43
8.5.2 Conversion of SR to D Flip-Flop 8.44
8.5.3 Conversion of SR to T Flip-Flop 8.45
8.5.4 Conversion of JK Flip-Flop to SR, D and T Flip-Flops 8.46
8.5.5 Conversion of D to SR Flip-Flop 8.46
8.5.6 Conversion of D to JK Flip-Flop 8.48
8.5.7 Conversion of D to T Flip-Flop 8.49
8.5.8 Conversion of T to SR Flip-Flop 8.50
8.5.9 Conversion of T to JK Flip-Flop 8.51
8.5.10 Conversion of T to D Flip-Flop 8.53

8.6 Summary of Important Concepts 8.68
8.7 Short-Answer Questions 8.69
8.8 Exercises 8.70

Chapter 9: Synchronous Sequential Circuits 9.1–9.84

9.1 Introduction 9.1
9.2 Analysis and Design of Synchronous (or Clocked) Sequential Circuits 9.2
9.2.1 Design of Mealy and Moore Models 9.2
9.3 State and State Equations 9.3
9.3.1 State Table and State Diagram 9.4
9.3.2 State Reduction 9.5
9.3.3 State Assignment 9.6
9.3.4 Lock-out Condition Circuit Implementation 9.7
9.4 Implementation of Sequential Logic Design using Standard IC's 9.68
9.5 Summary of Important Concepts 9.73
9.6 Short-Answer Questions 9.74
9.7 Exercises 9.75

Chapter 10: Sequential Logic-Counters and Registers 10.1–10.132

10.1 Design of Counters 10.1
10.2 Asynchronous or Ripple Counter 10.2
10.2.1 Up Counter 10.2
10.2.2 Down Counter 10.4
10.2.3 Up/Down Counter using T Flip-Flop 10.6
10.2.4 Down Counter with Positive Clock 10.7
10.2.5 BCD Counter 10.8
10.2.6 MOD Counter 10.11
10.3 Synchronous Counter 10.15
10.3.1 Synchronous Binary Up Counter 10.16
10.3.2 Synchronous Binary Down Counter 10.19
10.3.3 Synchronous Up/Down Counter 10.21
10.3.4 Synchronous BCD Counter 10.22
10.3.5 Ring Counter 10.26
10.3.6 Johnson Counter 10.27
10.3.7 Application of Counter 10.102
10.4 Implementation of Counters using Standard ICs 10.102
10.5 Register 10.109
10.6 Shift Register 10.111
10.6.1 Serial-in Serial-out Shift Register 10.111
10.6.2 Serial-in Parallel-out Shift Register 10.114
10.6.3 Parallel-in Serial-out Shift Register 10.114
10.6.4 Parallel-in Parallel-out Shift Register 10.115
10.6.5 Universal Shift Register 10.115
10.6.6 Application of Shift Register 10.119

10.7 Synchronous Systems Model Development 10.120
10.7.1 Designing of Rolling Display 10.121
10.7.2 Designing of Real Time Clock 10.121
10.8 Summary of Important Concepts 10.123
10.9 Short-Answer Questions 10.124
10.10 Exercises 10.126

Chapter 11: Asynchronous Sequential Circuits 11.1–11.110

11.1 Introduction to Asynchronous Sequential Logic Circuits 11.1
11.1.1 Fundamental and Pulse Mode Sequential Circuits 11.2
11.1.2 Transition Table 11.2
11.1.3 Stable and Unstable States 11.5
11.1.4 Flow Table 11.6
11.1.5 Cycles and Races 11.6
11.1.6 Race-Free Assignment 11.25
11.1.7 Transition Diagram 11.26
11.2 State Reduction 11.32
11.2.1 Implication Table 11.33
11.2.2 Merger Diagram to find Equivalent State Groups 11.36
11.2.3 Merging of Rows of Flow Tables with Incompletely Specified States 11.42
11.2.4 Merger Diagram to find Maximum Compatible States 11.42
11.2.5 Maximum Compatible 11.43
11.2.6 Closed-Covering Condition 11.43
11.2.7 Assigning Outputs in Flow Table with Incompletely Specified States 11.43
11.3 Asynchronous Circuits with SR Latches 11.52
11.3.1 NOR based SR Latch 11.52
11.3.2 NAND based SR Latch 11.53
11.3.3 Design using SR Latches 11.54
11.4 Design of Pulse Mode Asynchronous Sequential Circuits 11.72
11.5 Summary of Important Concepts 11.90
11.6 Short-Answer Questions 11.92
11.7 Exercises 11.97

Chapter 12: Hazards 12.1–12.50

12.1 Hazards 12.1
12.2 Hazards in Combinational Circuits 12.1
12.2.1 Static-0 and Static-1 Hazards 12.1
12.2.2 Dynamic Hazard 12.6
12.3 Hazards in Sequential Circuits 12.7
12.4 Essential Hazards 12.7
12.5 Design of Hazard Free Circuits 12.12
12.5.1 Elimination of Hazards in Combinational Circuits 12.12
12.5.2 Elimination of Hazards in Sequential Circuits 12.18
12.6 Summary of Important Concepts 12.39
12.7 Short-Answer Questions 12.40
12.8 Exercises 12.41

CHAPTER 13: Logic Families **13.1–13.74**

13.1 Logic Families 13.1
13.1.1 Evolution of Logic Family 13.1
13.2 Operation and Characteristics of Digitial Logic Families 13.2
13.2.1 Logic Levels 13.2
13.2.2 Propagation Delay 13.3
13.2.3 Power Requirement 13.4
13.2.4 Fan-out and Fan-in 13.5
13.2.5 Noise Margin 13.5
13.2.6 ON-OFF Characteristics of Bipolar Junction Transistors 13.7
13.2.7 ON-OFF Characteristics of CMOS Field Effect Transistors 13.8
13.3 RTL (Resistor-Transistor Logic) 13.10
13.3.1 RTL NOR Gate 13.10
13.3.2 RTL OR Gate 13.11
13.3.3 RTL NAND Gate 13.12
13.3.4 RTL AND Gate 13.14
13.3.5 RTL NOT Gate 13.15
13.4 DTL (Diode-Transistor Logic) 13.15
13.4.1 DTL NAND Gate 13.15
13.4.2 DTL NOR Gate 13.17
13.4.3 DTL NOT Gate 13.18
13.4.4 DTL AND Gate 13.19
13.4.5 DTL OR Gate 13.20
13.5 TTL (Transistor-Transistor Logic) 13.20
13.5.1 Types of Output in TTL Devices 13.20
13.5.2 TTL NAND Gate 13.22
13.5.3 TTL NOT Gate 13.24
13.5.4 TTL AND Gate 13.25
13.5.5 TTL NOR Gate 13.25
13.5.6 TTL OR Gate 13.27
13.6 ECL (Emitter Coupled Logic) 13.27
13.6.1 Emitter Coupled Current Switch 13.28
13.6.2 Emitter Coupled Basic Gate Circuit 13.29
13.6.3 ECL NOR Gate 13.33
13.6.4 ECL OR Gate 13.35
13.6.5 ECL NOT Gate 13.37
13.6.6 ECL NAND Gate 13.38
13.6.7 ECL AND Gate 13.41
13.7 CMOS (Complementary MOSFET) 13.43
13.7.1 CMOS NOT Gate 13.44
13.7.2 CMOS NOR Gate 13.44
13.7.3 CMOS OR Gate 13.46
13.7.4 CMOS NAND Gate 13.47
13.7.5 CMOS AND Gate 13.48

13.7.6 Buffered and Unbuffered CMOD Devices 13.49
13.7.7 Combinational Logic Implementation in CMOS 13.49
13.8 Comparison of Logic Families 13.60
13.8.1 Resistor-Transistor Logic (RTL) Family 13.61
13.8.2 Diode-Transistor Logic (DTL) Family 13.61
13.8.3 Transistor-Transistor Logic (TTL) Family 13.62
13.8.4 Emitter-Coupled Logic (ECL) Family 13.63
13.8.5 Complementary MOSFET Logic (CMOS) Family 13.63
13.9 Summary of Important Concepts 13.64
13.10 Short-Answer Questions 13.66
13.11 Exercises 13.68

CHAPTER 14: Memory and Programmable Logic Devices 14.1–14.78

14.1 Basic Concepts of Memory 14.1
14.1.1 Types of Semiconductor Memories 14.2
14.1.2 Functional Block Diagram of Semiconductor Memory 14.3
14.1.3 Memory or Binary Cell (BC) 14.5
14.1.4 Address Decoding in Memory 14.7
14.1.5 Address Multiplexing in Memory 14.8
14.2 ROM and PROM 14.11
14.2.1 Custom or Mask Programmed ROM 14.11
14.2.2 Programmable or Field Programmable ROM 14.12
14.2.3 EPROM 14.13
14.2.4 EEPROM/EAPROM 14.16
14.3 RAM 14.17
14.3.1 Static RAM 14.17
14.3.2 DRAM 14.21
14.3.3 Content-Addressable Memory (CAM) 14.23
14.4 Programmable Logic Devices 14.27
14.5 PROM as PLD 14.27
14.6 PLA (Programmable Logic Array) 14.31
14.6.1 Implementation of Combinational Circuit using PLA 14.33
14.7 PAL (Programmable Array Logic) 14.44
14.7.1 Implementation of Combinational Circuit using PAL 14.46
14.8 Sequential Programmable Logic Device (SPLD) 14.53
14.9 Complex Programmable Logic Device (CPLD) 14.54
14.10 Field Programmable Gate Array (FPGA) 14.55
14.10.1 Basic Architecture of FPGA 14.55
14.10.2 Xilinx FPGA Family of Devices 14.58
14.10.3 Spartan-6 Family of FPGA 14.58
14.10.4 Spartan-6 FPGA Architecture 14.60
14.11 Summary of Important Concepts 14.63
14.12 Short-Answer Questions 14.64
14.13 Exercises 14.69

CHAPTER 15: Data Converters **15.1–15.30**

15.1 Introduction 15.1
15.1.1 Parameters of Data Converters 15.2
15.2 Digital to Analog Converter (DAC) 15.3
15.2.1 R-2R Ladder Type DAC 15.4
15.2.2 Weighted-Resistor Type DAC 15.5
15.2.3 Switched Current-Source Type DAC 15.6
15.2.4 Switched Capacitor Type DAC 15.7
15.2.5 DAC0800 15.9
15.3 Analog to Digital Converter (ADC) 15.10
15.3.1 Flash Type ADC 15.11
15.3.2 Counter Type ADC 15.13
15.3.3 Tracking Type ADC 15.14
15.3.4 Dual-Slope Type ADC 15.15
15.3.5 Successive-Approximation Type ADC 15.16
15.3.6 ADC0809 15.17
15.4 Summary of Important Concepts 15.22
15.5 Short-Answer Questions 15.23
15.6 Exercises 15.26

APPENDICES **A1– A20**

APPENDIX 1: List of Some Standard IC's A.1
APPENDIX 2: Pin Configuration of Some Standard IC's A.2
APPENDIX 3: Summary of Various Binary Codes A.12
APPENDIX 4: Unsigned and Signed Binary Number System A.14
APPENDIX 5: Boolean Theorems A.15
APPENDIX 6: Two Variable Boolean Function A.16
APPENDIX 7: Summary of Flip-Flop Tables A.17
APPENDIX 8: List of Xillinx FPGAs A.18
APPENDIX 9: Spartan-6 FPGA Feature and Logic Resources A.20

UNIVERSITY QUESTION PAPERS **Q.1–Q.46**

INDEX **I.1– I.5**